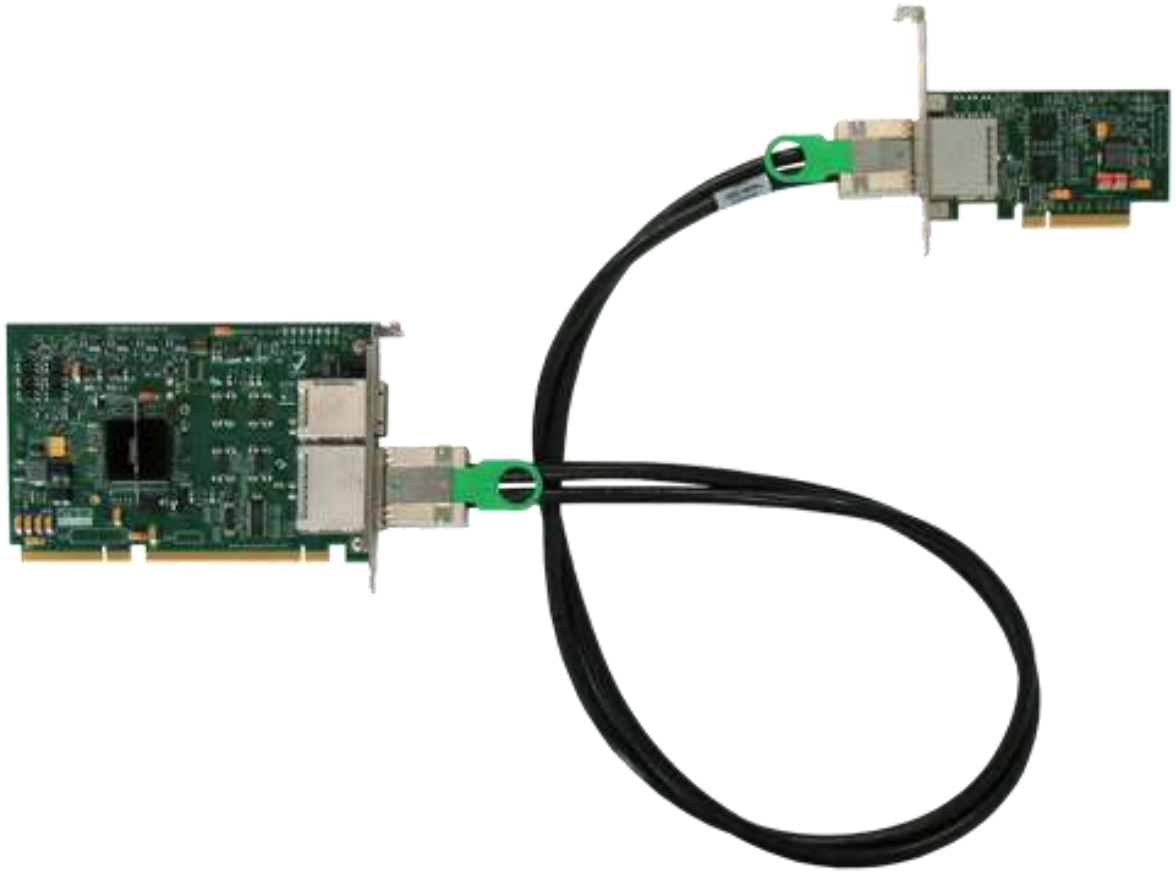

User Manual,
Expansion Kit, Server to SHB Backplane

(OSS-KIT-EXP-7500)

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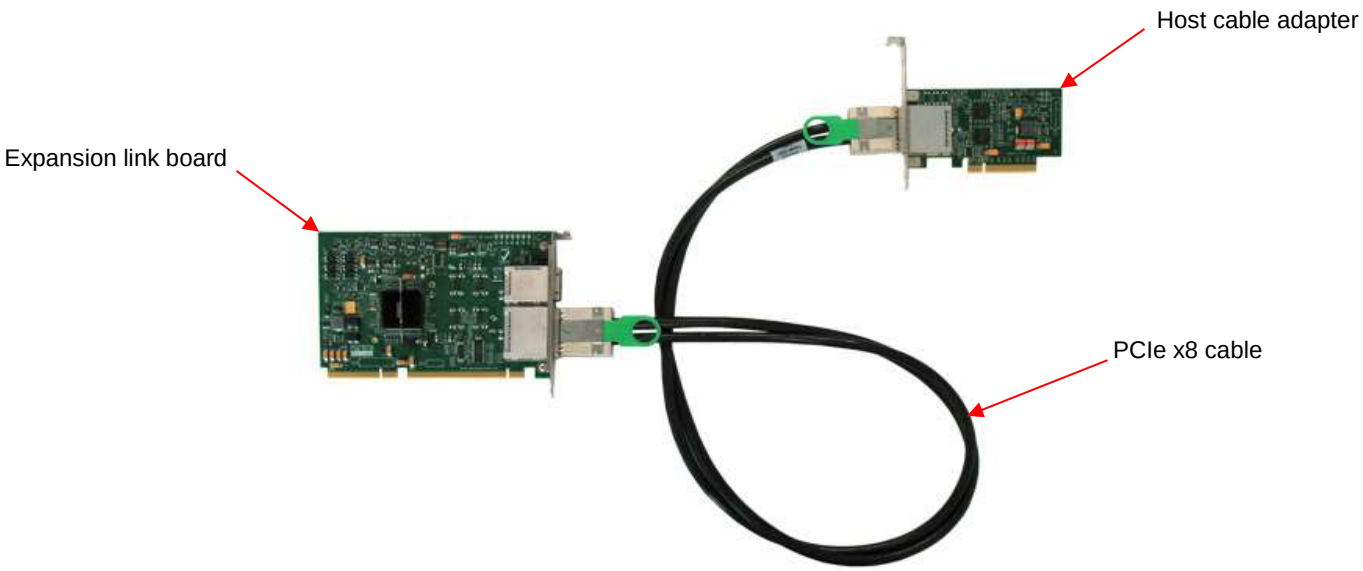
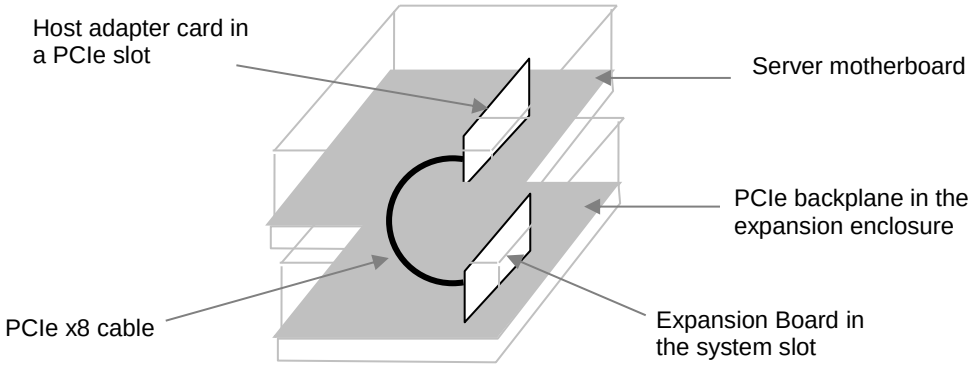
1.a. Description

The PCIe x8 Gen 2 expansion kit is used to extend the PCI express bus from a host server to an external expansion chassis. The host adapter card installs into a PCIe x8, or x16 slot of the server motherboard. It then cables to a downstream expansion board and installs in the SHB slot of the backplane and provides primary fan-out switch to support multiple configurations of PCI express expansion slots.

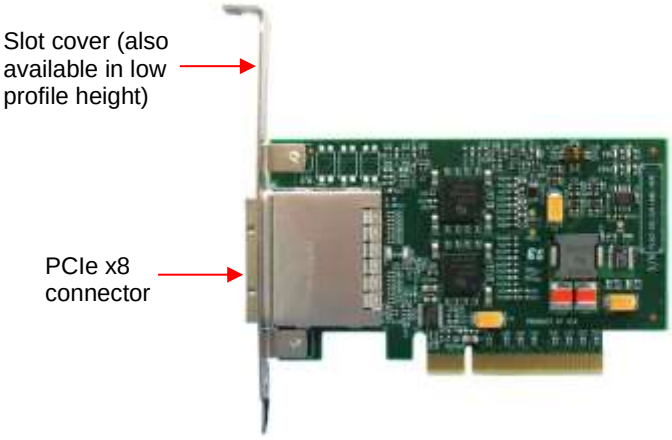


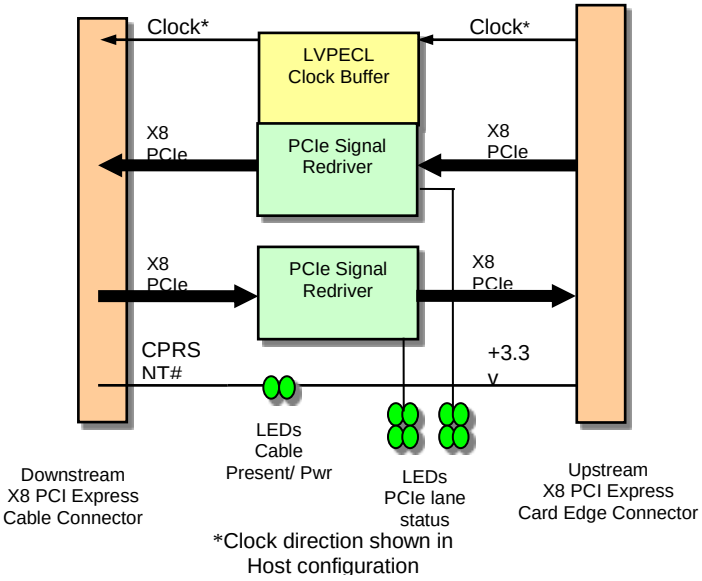

Host adapter card in a PCIe slot
Server motherboard
PCIe backplane in the expansion enclosure
PCIe x8 cable
Expansion Board in the system slot

2. Components

2.a. Host cable adapter

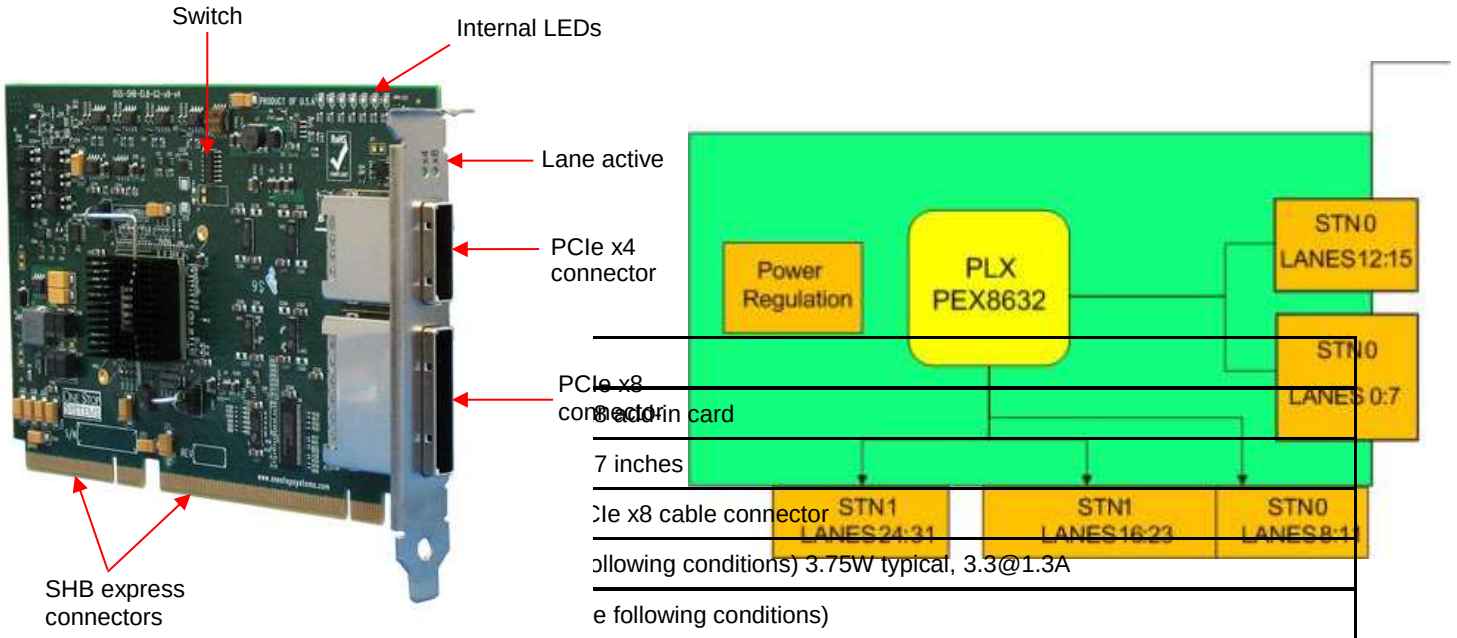
The PCIe x8 host adapter inserts into the host computer's PCIe x8 or x16 slot.





2.b. Expansion link board

The expansion link board installs in the extending or system host PCIe goes to all available slots on the expansion backplane and can control multiple configurations of PCIe expansion slots.



	8 add-in card
	7 inches
	CIe x8 cable connector
	llowing conditions) 3.75W typical, 3.3@1.3A
	e following conditions)
Temperature Range:	0° to 50°C (32° to 122°F)
Relative Humidity:	10 to 90% non-condensing
Shock:	30g acceleration peak (11ms pulse)
Vibration:	5-17 Hz 0.5" double amplitude displacement; 7-2000Hz, 1.5g acceleration.

2.c. **Host**

Redriver: Pericom PI2EQX5804
Agency Compliance: UL60950.FCC Class B, CE safety and emissions

Adapter Specifications

2.d. Expansion link board specifications

Form Factor	• PIC1.3 G SHB Express system slot compliant
Slot Type	System slot for the expansion chassis
Dimensions (H x L)	4.375 x 6.600 in (111 x 161 mm) 1 slot wide
Switch	PLX PEX8632 32 lane switch
Upstream Interface	x8 PCI Express over cable
Downstream Interface	20 lanes of PCI Express are auto configurable on the card edge connectors as: • One x16 and one x4 PCIe links • Two x8 and one x4 PCIe links • Five x4 PCIe links
Front Panel Connector	Molex 75586-0007(x8) and 75586-0010(x4)
Front Panel Indicators	• 8 Upstream Lane Active Indicators (Green)
Internal Indicators	• Power In-range Indicators for +12V, +3.3V & VTT (Red/Green) • Power on indicator for +1V (Green) • Bank of 5 board status indicators (Red)
Optional Features	• Switch Control: 3 banks of DIP switches for PEX8632 configuration • Switch Debug Port: Internal JTAG communications header • Heat Sink:On-board fan header provided for optional heat sink fan
Power Consumption	• 9W typical, 11.4W max • +12V @ 0.675A max, 3.3V @ 1.0 A max, 5Vaux @ 2.5mA max
Designed to meet the following	• Temperature Range:0° to 55 °C (32° to 122°F) • Relative Humidity:10 to 90% non-condensing • Shock:30g acceleration peak (11ms pulse) • Vibration: 5-17 Hz 0.5” double amplitude displacement; 7-2000Hz, 1.5g acceleration • Pending Compliance:UL 60950, FCC Class B, CE safety and emissions

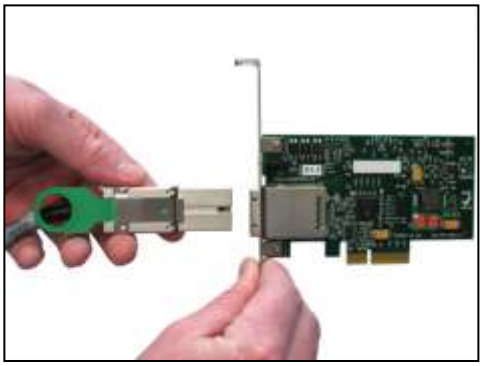
3. Installation Instructions

3.a. Installing the Adapter Kit

1) Install the host cable adapter into an appropriate PCIe slot of the host computer. NOTE: For example, a PCIe x8 host board can be installed in a PCIe x16 or a x8 slot. It will still operate at x8 speeds.

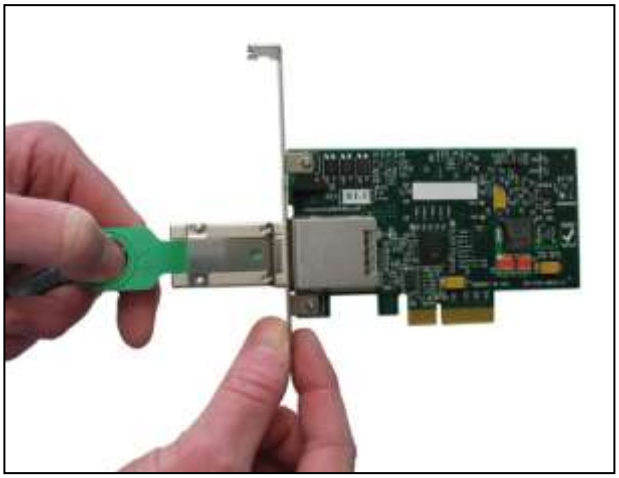
3.b. Installing the expansion link board:

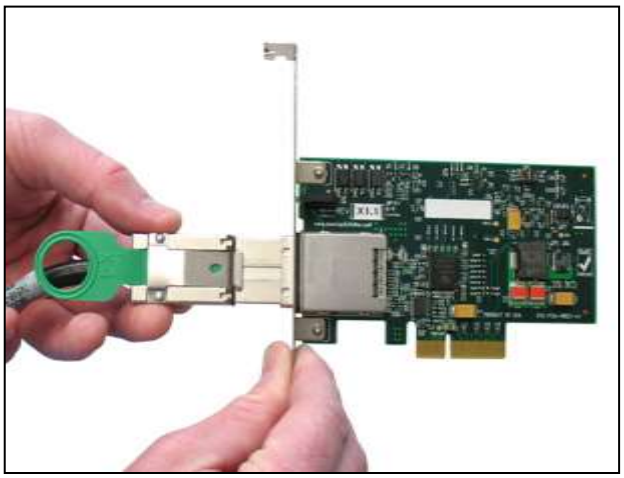
2) Insert the expansion link board into the SHB slot on the chosen backplane.
3) Connect the PCIe cable to both cable adapters.
    a) Pull back on the tab, lifting the prongs that insert in the holes on the PCIe connector.
    b) Push in the connector.
    c) Release green thumb tab insuring that the prongs are fully engaged in the mating connector.
    d) Test by pulling back on the connector.



3.c. Removing PCIe cable:

1) To remove PCIe cable pull back on green thumb tab to release metal pins and gently separate.





Operation:

1) Plug in expansion system and turn the power supply on.
2) Power up
3) The expansion system will power up

4. Technical Information

The transmit and receive signals on the OSS-HIB25-x8 are driven and conditioned by Pericom redriver chips. Adjustments can be made to equalization, de-emphasis and output swing. These controls are factory set by the use of zero Ohm resistors. In the following tables a 0 indicates that a zero Ohm resistor has been installed and a 1 indicates no resistor. In rare cases, mostly where non-OSS equipment is used with the OSS-HIB25-x8, these adjustments may need to be changed. The following tables are made available for this purpose. It is highly recommended to contact OSS customer support before making changes to these settings.

4.a. Signal Adjustment for the host cable adapter

Equalizer Selection

SEL_ 2[A:D]	SEL_ 1[A:D]	SEL_ 0[A:D]	@1.25 GHZ	@2.5 GHZ	
0	0	0	0.5dB	1.2dB	Edge Default
0	0	1	0.6dB	1.5dB	
0	1	0	1.0dB	2.6dB	
0	1	1	1.9dB	4.3dB	
1	0	0	2.8dB	5.8dB	
1	0	1	3.6dB	7.1dB	Cable Default
1	1	0	5.0dB	9.0dB	
1	1	1	7.7dB	12.3B	

De-emphasis Adjustment

D2_[A:D]	D1_[A:D]	D0_[A;D]	De-emphasis	
0	0	0	0dB	SW=ON Default
0	0	1	-2.5dB	
0	1	0	-3.5dB	
0	1	1	-4.5dB	
1	0	0	-5.5dB	
1	0	1	-6.5dB	SW=OFF Default
1	1	0	-7.5dB	
1	1	1	-8.5dB	

Output Swing Control

S_1[A:D]	S_0[A:D]	Swing (Diff. VPP)	
0	0	1V	Cable Default
0	1	05V	
1	0	0.7V	Edge Default
1	1	0.9V	

4.b. Pin Assignments

Host card connectors PCIe x8 Card Edge Connector

- The pins are numbered as shown with side A on the top of the centerline on the solder side of the board and side B on the bottom of the centerline on the component side of the board.
- The PCIe interface pins PETpx, PETnx, PERpx, and PERnx are named with the following convention: “PE” stands for PCIe high speed, “T” for Transmitter, “R” for Receiver, “p” for positive (+), and “n” for negative (-).
- Note that adjacent differential pairs are separated by two ground pins to manage the connector crosstalk.

Pin-out for the PCIe x8 Card Edge Connector on the Host Cable Adapter

Pin #	Side B		Side A	
	Name	Description	Name	Description
1	+12V	12V Power	PRSNT1#	Hot-Plug presence detect
2	+12V	12V Power	+12V	12V Power
3	+12V	12V Power	+12V	12V Power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI (Test Data Input)
7	GND	Ground	JTAG4	TDO (Test Data Output)
8	+3.3V	3.3 V power	JTAG5	TMS (Test Mode Select)
9	JTAG1	TRST# (Test Reset)	+3.3V	3.3 V power
10	3.3Vaux	3.3 V auxiliary power	+3.3V	3.3 V power
11	WAKE#	Signal for link reactivation	PERST#	Fundamental reset
Mechanical key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Transmitter differential pair, Lane 0	REFCLK	
15	PETn0		GND	Ground
16	GND	Ground	PERp0	Receiver differential pair, Lane 0
17	PRSNT2#	Hot-Plug presence detect	PERn0	
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential pair, Lane 1	RSVD	Reserved
20	PETn1		GND	Ground
21	GND	Ground	PERp1	Receiver differential pair, Lane 1
22	GND	Ground	PERn1	
23	PETp2	Transmitter differential pair, Lane 2	GND	Ground
24	PETn2		GND	Ground
25	GND	Ground	PERp2	Receiver differential pair, Lane 2
26	GND	Ground	PERn2	
27	PETp3	Transmitter differential pair, Lane 3	GND	Ground
28	PETn3		GND	Ground
29	GND	Ground	PERp3	Receiver differential pair, Lane 3
30	RSVD	Reserved	PERn3	

31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETp4	Transmitter differential pair, Lane 4	RSVD	Reserved
34	PETn4		GND	Ground
35	GND	Ground	PERp4	Receiver differential pair, Lane 4
36	GND	Ground	PERn4	
37	PETp5	Transmitter differential pair, Lane 5	GND	Ground
38	PETn5		GND	Ground
39	GND	Ground	PERp5	Receiver differential pair, Lane 5
40	GND	Ground	PERn5	
41	PETp6	Transmitter differential pair, Lane 6	GND	Ground
42	PETn6		GND	Ground
43	GND	Ground	PERp6	Receiver differential pair, Lane 6
44	GND	Ground	PERn6	
45	PETp7	Transmitter differential pair, Lane 7	GND	Ground
46	PETn7		GND	Ground
47	GND	Ground	PERp7	Receiver differential pair, Lane 7
48	PRSNT2#	Hot-Plug presence detect	PERn7	
49	GND	Ground	GND	Ground

Notes:

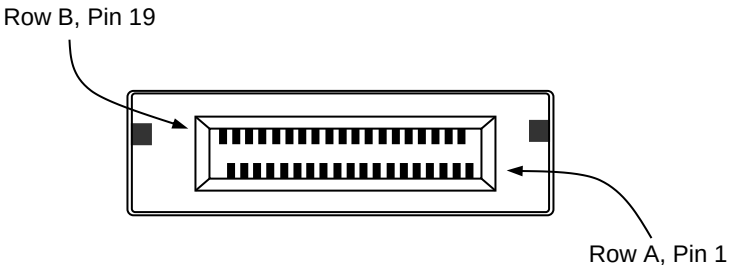
1. Optional signals that are not implemented are left as no connects on the board side connector.

2. Reserved signals are no connects on the board side connector.

3. Although support of CWAKE# is optional from the board side connector perspective, an allocated wire is mandated for the cable assembly.

4. Board side pin-outs on both sides of the Link are identical. The cable assembly incorporates a null modem for the PCIe transmit and receive pairs.

4.c. PCI Express x8 Connector Pin Assignment



4.d. Pin-out for the PCIe x8 Cable

	Row A	Row B		Row A	Row B		Row A	Row B
Pin #	Signal Name	Signal Name	Pin #	Signal Name	Signal Name	Pin #	Signal Name	Signal Name
1	GND	GND	13	GND	GND	24	PETn4	PERp4
2	PETp0	PERp0	14	CREFCLK+	PWR (3.3V)	25	GND	GND
3	PETn0	PERn0	15	CREFCLK-	PWR (3.3V)	26	PETp5	PERp5
4	GND	GND	16	GND	PWR (3.3V)	27	PETn5	PERn5
5	PETp1	PERp1	17	RSVD	PWR RTN	28	GND	GND
6	PETn1	PERn1	18	RSVD	PWR RTN	29	PETp6	PERp6
7	GND	GND	19	SB_RTN	PWR RTN	30	PETn6	PERn6
8	PETp2	PERp2	20	CPSRNT$#	CWAKE#	31	GND	GND
9	PETn2	PERn2	21	CPWRON	CPERST#	32	PETp7	PERp7
10	GND	GND	22	GND	GND	33	PETn7	PERn7
11	PETp3	PERp3	23	PETp4	PETp4	34	GND	GND
12	PETn3	PERn3	24	PETn4	PERp4			

4.e. Signal Descriptions

PETp(x)	PCI Express Transmit Positive signal of (x) pair.
PETn(x)	PCI Express Transmit Negative signal of (x) pair.
PERp(x)	PCI Express Receive Positive signal of (x) pair.
PERn(x)	PCI Express Receive Negative signal of (x) pair.
CREFCLK+/-	Cable REFerence CLocK: Provides a reference clock from the host system to the remote system.
SB_RTN	Side Band ReTurN: return path for single ended signals from remote systems.
CPRSNT#	Cable PReSeNT: Indicates the presence of a device beyond the cable.
PWR	PoWeR: Provides local power for in-cable redriver circuits. Only needed on long cables. Power does not go across the cable.)
PWR_RTN	PoWeR ReTurN: Provides local power return path for PWR pins.
CWAKE#	Cable WAKE
CPERST#	Cable PCI Express Reset

4.f. Expansion link board switch settings

Downstream PCIe ports hardware strapping logic

CFG(0:2)			BP PORT CFG				
0	1	2	A0	A1	A2	A3	B0
0	0	0	x4	x4	x4	x4	x4
0	1	0	x8	0	x4	x4	x4
0	1	1	x8	0	x8	0	x4
1	x	x	x16	0	0	0	x4

5. Ordering Information

OSS-KIT-EXP-7500

PCIe x8 Gen 2 expansion kit includes a PCIe x8 Gen 2 host cable adapter, a PCIe x4/x8 expansion link board, and a PCIe x8 2M cable.